High Thermal Efficiency Modeling Technique for High Power LED Packages

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High-power, high-brightness LEDs are penetrating an increasing number of lighting applications because of their excellent color saturation and long life characteristics.

With the ever-increasing combination of higher heat flux with higher package density in high-power LEDs, providing sufficient heat dissipation from the LED package module is becoming increasingly challenging, which makes effective thermal analysis and design more important. Computational fluid dynamic (CFD) modeling of LED components has become an extremely useful tool in the application design process. CFD modeling is concerned with the numerical simulation of fluid flow, heat transfer and other related processes such as radiation.

This article presents work that was done to create a high-power LED star package assembly with a heat sink that is capable of maintaining the junction temperature of a nominal one-watt LED light source that operates at 3.5 V and 350 mA (typical) to the maximum value of 125ºC.

First, a detailed model of an LED package mounted on a star substrate is created, and then the model is modified to show a heat sink on the bottom of the LED star package assembly. Finally, resulting simulation data is compared to experimental data on the assembly. A focus of this article is an examination of the effects of different thermal interface materials (TIMs), bond line thicknesses and percentages of trapped voids in the TIM on the thermal performance of the LED star assembly.

Thermal Modeling Technique

The LED package itself, the package assembled on a star substrate metal-core printed circuit board (MCPCB), and the star substrate assembly bonded to a heat sink were modeled using Flotherm, which is a CFD tool from Flomerics Group PLC.

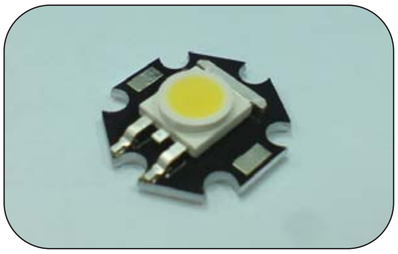

Figure 1. Isometric view of Avago's Moonstone Power LED Star package (ASMT-Mx09)

A detailed model was developed to allow the comparison of error percentages to actual measurements on the assembly. An isometric view of the LED star package assembly is shown in Figure 1. The gap between the package and substrate is filled with solder paste. When the package reaches the maximum operating power of 1.3 watts, natural and forced-convection air cooling cannot maintain the LED junction temperature within the acceptable range of 125ºC maximum, which calls for the addition of a heat sink. To mount the heat sink onto the star substrate, an adhesive thermal tape is attached to the backside of the heat sink, and the heat sink affixed to the bottom of the substrate.

Grid and Boundary Conditions

For CFD analysis, the following properties are assumed: three dimensional, steady state, still air, air properties are constant, ambient temperature is 25°C, computational domain is 305 mm by 305 mm by 305 mm, and heat is dissipated through a combination of natural convection, conduction and radiation.

The total number of grid cells for the LED package-on-substrate and the detailed heat sink model is about 200,000. For the grid cell setup, it is recommended that at least three cells be used between the fins of the heat sink.

Thermal Resistance Calculation

To calculate the thermal resistance of the heat flowing vertically through the LED die, the die attach (DA) layers, die pad, TIM, heat sink and dielectric layer to the substrate are measured. With each layer having its own thermal properties, the thermal resistance from the die junction to the ambient, R_{JA}, can be calculated by using the following equations:

$$R_{JA} = R_{J\text{-}MS} + R_{MS\text{-}A} \qquad (1)$$

$$R_{MS\text{-}A} = (T_{MS} - T_A) / Power \qquad (2)$$

Where $R_{J\text{-}MS}$ = 10°C/W (Refer to ASMT-MW09 data sheet)

The R_{JA} represents how well the heat is dissipated from the LED chip junction to the ambient temperature, with a lower value of R_{JA} resulting in better thermal performance. To help to understand the entire combination of thermal paths involved, Figure 2 shows 2D views of the cross section of the package structures.

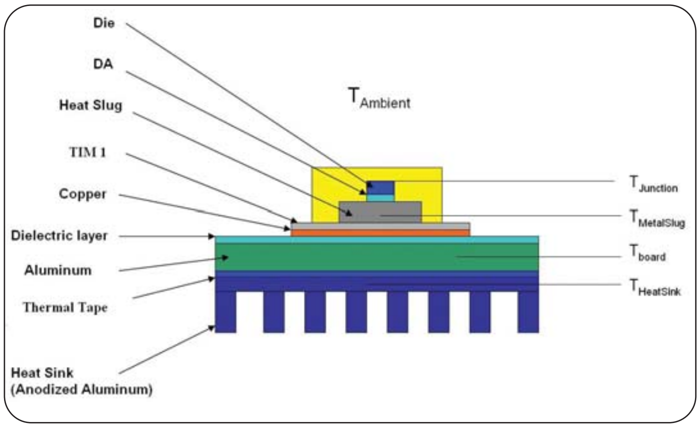

Figure 2. 2D views of the cross section of the package structures.

The LED package is mounted on a star MCPCB. The heat sink, which is a typical finned-type with 110 fins and a base made of extruded aluminum, is attached to the back of the star MCPCB with thermal tape. The package is driven at 1.2 W and the temperature of the solder point (TMetalSlug) is measured with a thermocouple at the metal slug of the package (Refer to Figure 3). The measurement is only taken after temperature saturation is reached.

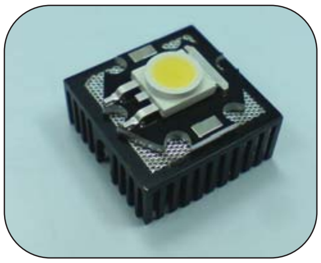

Figure 3. Temperature measurement point on Moonstone LED package.

A comparison of the measured data to the simulation model is shown in Table 1, with simulation visualization results shown in Figures 4a and 4b. Since the simulated temperature is higher than the measured temperature, it indicates that the numerical model failed to account for the amplitude of some of the cooling phenomena.

	Measured RJA (oC/W)	Simulated RJA (oC/W)	Error (%)
LED package on Star MCPCB without heat sink	44	47	6
LED package on Star MCPCB with heat sink	28	30	7

Table 1. Simulated Results vs. Measured Results.

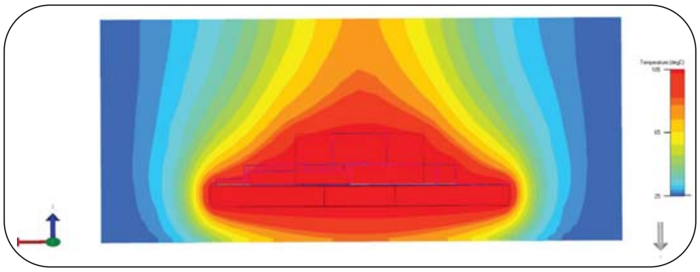

Figure 4a. Visualization results for LED star package assembly

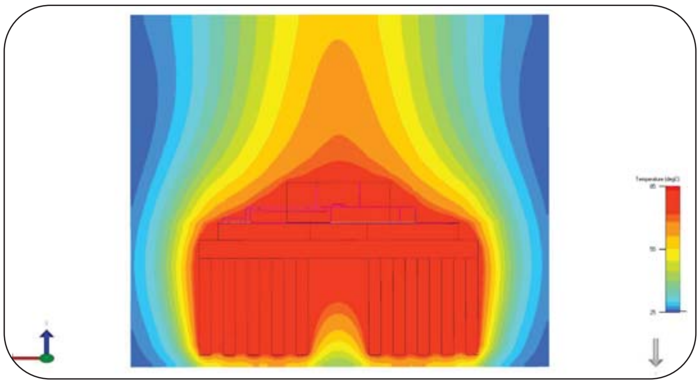

Figure 4b. Visualization result for LED package on MCPCB with detailed heat sink model.

Impact of the Thermal Interface Material

The thermal interface material (TIM) plays a key role in carrying the heat from the LED package to the board or heat sink. In Figure 2, TIM 1 is located between the LED package and substrate.

The effects of increasing thermal conductivity of TIM 1 on the interface thermal resistance, as the bond line thickness increases between the LED package and substrate with heat sink. The numerical simulation results show that the thermal resistance is more sensitive to TIM thermal conductivity as the bond line thickness increases, and that the impact of different thermal conductivity values and different bond line thickness is not overly significant.

Any air gap between two non-conforming solid surfaces will reduce thermal conductivity. A function of the TIM is to conform to the microscopic surface contours of the adjacent solid surfaces and increase the area of contact between the LED package metal slug (heat source), and the metal core PCB (heat sink). As a result, the TIM is able to reduce the temperature drop across this contact. The R_{JA} estimates in Figure 5 are the result of a numerical simulation study of the effect of TIM 1 contact quality on thermal performance. A single void resulting from the manufacturing process is assumed to form at the center region of the total volume.

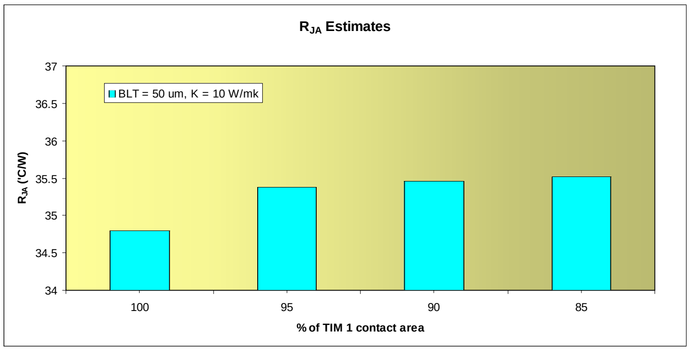

Figure 5. The effect on RJA of various TIM 1 contact area percentages.

The maximum R_{JA} increase is estimated at approximately 2 percent with an 85 percent contact area. The conclusion is that a void trapped inside the TIM 1 can represent up to 15 percent of the area without causing any significant reduction in thermal performance. It should be noted, though, that the predicted results have an error rate of up to 20 percent because of modeling assumptions, meaning that an experimental study is required to verify the numerical data.

Additional Thermal Design Considerations

Besides using TIM, thermal performance can be improved with attention to the following aspects of thermal design:

- Heat sink geometry, surface texture and orientation with respect to air flow
- System enclosure air flow path design to promote natural convection cooling
- Use of an active cooling system such as a fan or heat pipe to augment natural convection cooling

This article illustrated how the CFD modeling technique can be used for simulating an LED star package with a heat sink. The results clearly show that the results of the simulation model substantially agree with actual measurements. This means that CFD analysis is a good tool to assist the design engineer in using power LEDs in actual applications, with a percentage of error acceptable for industrial applications. The increase of thermal resistance is more sensitive to the area of contact than to the thermal conductivity of commercial TIM materials as the bond line thickness increases, and a trapped void within the TIM of up to 15 percent of the contact area will not cause any significant degradation of thermal performance.

Glossary of Terms

RJA	**Junction to ambient thermal resistance (oC/W)**
RJ-MS	**Junction to metal slug thermal resistance (oC/W)**
RMS-A	**Metal slug to ambient thermal resistance (oC/W)**
TJ	**Junction temperature (oC)**
TMS	**Metal Slug (solder Point) temperature (oC)**
MCPCB	**Metal core printed circuit board**
TIM	**Thermal Interface Material**
BLT	**Bond Line Thickness**
CFD	**Computational Fluid Dynamics**

References

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